EXHIBIT 3A

Defendants' Statement of Issues of Fact That Remain to be Litigated

Defendants Fairchild Semiconductor Corporation and Fairchild Semiconductor International, Inc. (collectively, "Fairchild") expect to present the below listed issues of fact at the invalidity trial. To the extent that any issues of law set forth in Exhibit 5 of the Joint Pretrial Order may be considered issues of fact, Fairchild incorporates those portions of Exhibit 5 by reference.

1. Whether the Asserted Claims are invalid because they are anticipated under 35 U.S.C. § 102.

2. Whether the Asserted Claims are invalid because they are obvious under 35 U.S.C. § 103.

3. Whether the Asserted Claims are invalid because they fail to meet the requirements of 35 U.S.C. § 112.

4. The dates of conception and reduction to practice of the '075 Patent.

5. Whether the alleged inventor of the '075 Patent was both the first to conceive of the invention and thereafter exercised diligence between the conception of the invention of the '075 Patent and the filing of that patent on April 24, 1987.

6. The dates of conception and reduction to practice of the inventions of James Beasom, later disclosed and claimed in U.S. Patent No. 4,823,173.

7. Whether James Beasom, the inventor of U.S. Patent No. 4,823,173 abandoned, suppressed, or concealed his invention.

8. Whether Power Integrations added new matter during the prosecution of the '075 Patent.

Fairchild expects to present additional issues of fact during any hearing before the Court on equitable issues such as Power Integrations' inequitable conduct, whether an injunction is appropriate, whether any damages should be increased, and whether this case is exceptional. Fairchild will revise identification once the Court schedules such a hearing and identifies the issues to be considered. Fairchild anticipates, however, that the issues of fact to be litigated during any hearing on inequitable conduct will include (but not be limited to) Fairchild's intended proofs regarding inequitable conduct set forth in detail in Fairchild's February 23, 2006 First Amended Answer And Counterclaims To Plaintiff's First Amended Complaint For Patent Infringement And Demand For Jury Trial. In addition, Fairchild will prove that Klas Eklund and Power Integrations intentionally failed to disclose at least the following material prior art, and otherwise failed to inform the patent office of material prior art as discussed during the June 7, 2007 deposition of Klas Eklund and in the documents produced by Klas Eklund in May 2007:

a. James D. Plummer, Monolithic MOS High Voltage Integrated Circuits, IEDM 80, pp. 70-74 (1980) (documents produced as Bates Nos. FCS0526740-FCS0526745)

b. Katsumasa Fujii, Yasuo Torimaru, Kiyotoshi Nakagawa, Takeo Fujimoto & Yoshimasa Aoki, Session III: Solid-State Devices WAM 3.6: 400V MOS IC for EL Display, ISSCC 81, pp. 46-47 (February 18, 1981)

c. Tadanori Yamaguchi & Seiichi Morimoto, Process And Device Design Of A 1000-Volt MOS IC, IEDM 81, pp. 255-258 (1981)

d. J. Tihanyi, Integrated Power Devices, IEDM 82, pp. 6-10 (1982)

e. Robert S. Wrathall, David Tam, Louis Terry, Integrated Circuits for the Control of High Power, IEDM 83, pp. 408-411 (1983)

f. Michael Pomper, Ludwig Leipold, Jeno Tihanyi & Hans-Eberhard Longo, IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 3, pp. 328-330 (June 1980)

g. Vladimir Rummennik, David L. Heald, Integrated High and Low Voltage CMOS Technology, IEDM 1982, pp. 77-80 (1982) (Eklund depo. exhibit 32

h. Bernard DesCamps, Jean-Claude Rufray, Session II: Consumer Circuits WAM 2.3: Integrated High-Voltage Video Amplifier for Color TV, ISSCC 81, pp. 28-29 (February 18, 1981)

i. A.R. Alvarez, R.M. roop, K.I. Ray, G.R. Gettemeyer, Lateral DMOS Transistor Optimized For High Voltage BIMOS Applications, IEDM 83, pp. 420-423 (1983)

j. Walter H.A. Mattheus, Session XVII: Telecommunication Circuits FAM 17.2: 400V Switches for Subscriber Line Interface, ISSCC 81, pp. 238-239 (February 20, 1981)

k. P.L. Hower, T.M.S. Heng, C. Huang, Optimum Design of Power MOSFETS, IEDM 83, pp. 87-90 (1983)

l. Sel Colak, Effects of Drift Region Parameters on the Static Properties of Power LDMOST, IEEE Transactions on Electron Devices, Vol. ED-28, No. 12, pp. 1455-1466 (December 1981) (Bates-labeled as FCS0526755-FCS0526767)13. H.M.J. Vaes, J.A. Appels, High Voltage, High Current Lateral Devices IEEE 1980, pp. 87-90 (1980) (produced as Bates Nos. FCS1693719-FCS1693724)

m. Power and logic devices are merging on the same chip, Computer Design (August 1984) (KE001518-KE001519 – "Texas BIDFET Approach")

n. Integrated Circuits Magazine article (March/April 1984) (KE001521-KE001522)

o. 400V transistor from NEC (KE001450)

p. 1000V transistor from Tektronix (KE001450)

q. 400V transistor from Philips (KE001450)

r. 200-400V devices for display driving from Sharp (KE001451)

s. 200-400V devices for display driving from Supertex (KE001451)

t. 200-400V devices for display driving from Siliconix (KE001451)

u. 200-400V devices for display driving from Telmos (KE001451)

v. 30-50V display drivers from AMI (KE001451)

w. 30-50V display drivers from Holt (KE001451)

x. Smartpower II D-MOS vertical transistor from Motorola (KE001451)

y. Smartpower I device from Motorola (KE001451)

z. Proposal from Xerox (KE001451-KE001452)

aa. 200V device from Thompson CSF (KE001452)

bb. BIDFET technology from Texas Instruments (KE001452)

cc. Bipolar high voltage transistors combined with low voltage CMOS from Motorola, Analog Devices, Sprauge and Unitrode (KE001452)

dd. Proposal from Philips (KE001453)

ee. Proposal from Motorola (KE001453)

ff. 400V switch for subscriber line interface from Bell (KE001453)

gg. 200V Supertex high voltage C-MOS approach for display drivers “open drain” (KE001520, KE001481)

hh. 90V Supertex high voltage C-MOS approach for display drivers “push and pull” (KE001520)

ii. Integrated DMOS device from SGS (KE001482)

jj. Lateral DMOS device from General Electric (KE001483)

kk. 250V DMOS in combination with 80 volt bipolar and low voltage CMOS from Texas Instruments (KE001570)

ll. 250V DMOS in combination with 80V bipolar from Thompson (KE001570)

mm. 200V DMOS in combination with low voltage CMOS from Supertex (KE001570)

nn. 100V DMOS in combination with low voltage CMOS from Siliconix (KE001570)

EXHIBIT 3B

Defendants' Statement of Intended Proofs

During the invalidity trial, Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation (collectively, "Fairchild") intend to prove the following:

1. The Asserted Claims are invalid because they are anticipated under 35 U.S.C. § 102.

2. The Asserted Claims are invalid because they are obvious under 35 U.S.C. § 103.

3. The Asserted Claims are invalid because they fail to meet the requirements of 35 U.S.C. § 112.

4. Power Integrations cannot prove that the '075 Patent was conceived and/or reduced to practice prior to April 24, 1987.

5. The addition of new matter during the prosecution of the '075 Patent results in that patent having a priority date of April 7, 1988.

6. Power Integrations cannot prove that Klas H. Eklund was both the first to conceive of the invention of claims 1 and 5 and thereafter was diligent between the conception of the invention of the '075 Patent and the filing of that patent on April 24, 1987.

7. U.S. Patent No. 4,823,173 was conceived and reduced to practice prior to the invention of the '075 Patent.

8. The invention of the '075 Patent was described in U.S. Patent No. 4,823,173, which is a patent granted on an application for patent by another filed in the United States before the invention by the applicant for the '075 Patent.

9. Before the invention of the '075 Patent, the invention was made in this country by James D. Beasom, who had not abandoned, suppressed, or concealed it.

10. Claims 1 and 5 of the '075 Patent are invalid pursuant to 35 U.S.C. §§ 102 and 103 in light of at least the following references and prior art, alone or in combination:

- James Beasom's prior conception and reduction to practice of the invention.
- U.S. Patent No. 4,823,173.
- H. Wakaumi, A Highly Reliable 16 Output High Voltage NMOS/CMOS Logic IC With Shielded Source Structure, IEDM 83, pp. 416-419 (1983).
- A. Ludikhuize, High-Voltage DMOS and PMOS in Analog IC's, IEDM 82, pp. 81-84 (1982).
- I. Wacyk, M. Amato & V. Rummennick, A Power IC with CMOS Analog Control (1986).

Fairchild will prove that none of these references were provided to the Examiner during the prosecution of the '075 Patent.

11. Claim 1 of the '876 Patent is invalid pursuant to 35 U.S.C. §§ 102 and 103 in light of at least the following references, alone or in combination:

- H. Martin, G. Hitler & D. Parsley, U.S. Patent No. 4,638,417, Power Density Spectrum Controller (Jan. 20, 1987).
- A. C. Wang & S. R. Sanders, Programmed Pulsewidth Modulated Waveforms for Electromagnetic Interference Mitigation in DC –DC Converters, IEEE Transactions on Power Electronics, Vol. 8, No. 4, pp. 596 – 605 (Oct. 1993).
- T. Habetler & D. Divan, Acoustic Noise Reduction in Sinusoidal PWM Drives Using a Randomly Modulated Carrier, IEEE Transactions on Power Electronics, Vol. 6, No. 3, pp. 356 – 363 (Jul. 1991).

Fairchild will prove that none of these references were provided to the Examiner during the prosecution of the '876 Patent.

12. Claims 1 and 4 of the '851 Patent are invalid pursuant to 35 U.S.C. §§ 102 and 103 in light of at least the following references, alone or in combination:

- SGS-Thompson's TEA2262 (as described in schematics, datasheets, and articles).
- H. Martin, G. Hitler & D. Parsley, U.S. Patent No. 4,638,417, Power Density Spectrum Controller (Jan. 20, 1987).
- A. C. Wang & S. R. Sanders, Programmed Pulsewidth Modulated Waveforms for Electromagnetic Interference Mitigation in DC –DC Converters, IEEE Transactions on Power Electronics, Vol. 8, No. 4, pp. 596 – 605 (Oct. 1993).
- T. Habetler & D. Divan, Acoustic Noise Reduction in Sinusoidal PWM Drives Using a Randomly Modulated Carrier, IEEE Transactions on Power Electronics, Vol. 6, No. 3, pp. 356 – 363 (Jul. 1991).
- Power Integrations' SMP3 (as described in schematics, datasheets, and articles).
- Power Integrations' SMP211 (as described in schematics, datasheets, and articles).
- Power Integrations' SMP240/260 (as described in schematics, datasheets, and articles).

Fairchild will prove that none of these references were provided to the Examiner during the prosecution of the '851 Patent.

13. Claims 9 and 14 of the '366 Patent are invalid pursuant to 35 U.S.C. §§ 102 and 103 in light of at least the following references, alone or in combination:

- Power Integrations' SMP3 (as described in schematics, datasheets, and articles).
- Power Integrations' SMP211 (as described in schematics, datasheets, and articles).
- Power Integrations' SMP240/260 (as described in schematics, datasheets, and articles).
- SGS-Thompson's TEA2262 (as described in schematics, datasheets, and articles).

- H. Martin, G. Hitler & D. Parsley, U.S. Patent No. 4,638,417, Power Density Spectrum Controller (Jan. 20, 1987).

- A. C. Wang & S. R. Sanders, Programmed Pulsewidth Modulated Waveforms for Electromagnetic Interference Mitigation in DC –DC Converters, IEEE Transactions on Power Electronics, Vol. 8, No. 4, pp. 596 – 605 (Oct. 1993).

- T. Habetler & D. Divan, Acoustic Noise Reduction in Sinusoidal PWM Drives Using a Randomly Modulated Carrier, IEEE Transactions on Power Electronics, Vol. 6, No. 3, pp. 356 – 363 (Jul. 1991).

Fairchild will prove that none of these references were provided to the Examiner during the prosecution of the '366 Patent.

14. "Programmed Pulsewidth Modulated Waveforms For Electromagnetic Interference Mitigation In DC-DC Converters" by A.C. Wang and S.R. Sanders was published in October 1993 in IEEE Transactions on Power Electronics, Vol. 8, No. 4.

15. "Acoustic Noise Reduction In Sinusoidal PWM Drives Using A Randomly Modulated Carrier" by T.G. Habetler and D.M. Divan was published in July 1991 in IEEE Transactions on Power Electronics, Vol. 6, No. 3, p. 356.

16. "A Highly Reliable 16 Output High Voltage NMOS/CMOS Logic IC With Shielded Source Structure" by H. Wakaumi was published in 1983 in IEDM 83, pp. 416-419.

17. "High-Voltage DMOS and PMOS in Analog IC's" by A. Ludikhuize was published in 1982 in IEDM 82, pp. 81-84.

18. "A Power IC with CMOS Analog Control" by I. Wacyk, M. Amato and V. Rummennick was published in 1986.

19. Power Integrations' SMP3, SMP211, and SMP240/260 were in public use or on sale and described in printed publications more than one year before May 18, 1998.

The SGS –Thompson TEA2262 device was in public use or on sale and described in printed publications more than one year before May 18, 1998.

20. Fairchild's intended proofs regarding inequitable conduct are set forth in detail in Fairchild's February 23, 2006 First Amended Answer And Counterclaims To Plaintiff's First Amended Complaint For Patent Infringement And Demand For Jury Trial. In addition, Fairchild will prove that Klas Eklund and Power Integrations intentionally failed to disclose at least the following material prior art, and otherwise failed to inform the patent office of material prior art as discussed during the June 7, 2007 deposition of Klas Eklund and in the documents produced by Klas Eklund in May 2007:

- James D. Plummer, Monolithic MOS High Voltage Integrated Circuits, IEDM 80, pp. 70-74 (1980) (documents produced as Bates Nos. FCS0526740-FCS0526745)

- Katsumasa Fujii, Yasuo Torimaru, Kiyotoshi Nakagawa, Takeo Fujimoto & Yoshimasa Aoki, Session III: Solid-State Devices WAM 3.6: 400V MOS IC for EL Display, ISSCC 81, pp. 46-47 (February 18, 1981)

- Tadanori Yamaguchi & Seiichi Morimoto, Process And Device Design Of A 1000-Volt MOS IC, IEDM 81, pp. 255-258 (1981)

- J. Tihanyi, Integrated Power Devices, IEDM 82, pp. 6-10 (1982)
- Robert S. Wrathall, David Tam, Louis Terry, Integrated Circuits for the Control of High Power, IEDM 83, pp. 408-411 (1983)
- Michael Pomper, Ludwig Leipold, Jeno Tihanyi & Hans-Eberhard Longo, IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 3, pp. 328-330 (June 1980)
- Vladimir Rummennik, David L. Heald, Integrated High and Low Voltage CMOS Technology, IEDM 1982, pp. 77-80 (1982) (Eklund depo. exhibit 32
- Bernard DesCamps, Jean-Claude Rufray, Session II: Consumer Circuits WAM 2.3: Integrated High-Voltage Video Amplifier for Color TV, ISSCC 81, pp. 28-29 (February 18, 1981)
- A.R. Alvarez, R.M. roop, K.I. Ray, G.R. Gettemeyer, Lateral DMOS Transistor Optimized For High Voltage BIMOS Applications, IEDM 83, pp. 420-423 (1983)
- Walter H.A. Mattheus, Session XVII: Telecommunication Circuits FAM 17.2: 400V Switches for Subscriber Line Interface, ISSCC 81, pp. 238-239 (February 20, 1981)
- P.L. Hower, T.M.S. Heng, C. Huang, Optimum Design of Power MOSFETS, IEDM 83, pp. 87-90 (1983)
- Sel Colak, Effects of Drift Region Parameters on the Static Properties of Power LDMOST, IEEE Transactions on Electron Devices, Vol. ED-28, No. 12, pp. 1455-1466 (December 1981) (Bates-labeled as FCS0526755-FCS0526767)13. H.M.J. Vaes, J.A. Appels, High Voltage, High Current Lateral Devices IEEE 1980, pp. 87-90 (1980) (produced as Bates Nos. FCS1693719-FCS1693724)
- Power and logic devices are merging on the same chip, Computer Design (August 1984) (KE001518-KE001519 – "Texas BIDFET Approach")
- Integrated Circuits Magazine article (March/April 1984) (KE001521-KE001522)
- 400V transistor from NEC (KE001450)
- 1000V transistor from Tektronix (KE001450)
- 400V transistor from Philips (KE001450)
- 200-400V devices for display driving from Sharp (KE001451)
- 200-400V devices for display driving from Supertex (KE001451)
- 200-400V devices for display driving from Siliconix (KE001451)
- 200-400V devices for display driving from Telmos (KE001451)
- 30-50V display drivers from AMI (KE001451)
- 30-50V display drivers from Holt (KE001451)

- Smartpower II D-MOS vertical transistor from Motorola (KE001451)
- Smartpower I device from Motorola (KE001451)
- Proposal from Xerox (KE001451-KE001452)
- 200V device from Thompson CSF (KE001452)
- BIDFET technology from Texas Instruments (KE001452)
- Bipolar high voltage transistors combined with low voltage CMOS from Motorola, Analog Devices, Sprauge and Unitrode (KE001452)
- Proposal from Philips (KE001453)
- Proposal from Motorola (KE001453)
- 400V switch for subscriber line interface from Bell (KE001453)
- 200V Supertex high voltage C-MOS approach for display drivers "open drain" (KE001520, KE001481)
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- Integrated DMOS device from SGS (KE001482)
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- 250V DMOS in combination with 80 volt bipolar and low voltage CMOS from Texas Instruments (KE001570)
- 250V DMOS in combination with 80V bipolar from Thompson (KE001570)
- 200V DMOS in combination with low voltage CMOS from Supertex (KE001570)
- 100V DMOS in combination with low voltage CMOS from Siliconix (KE001570)

Fairchild intends to offer additional proofs during any hearing before the Court on equitable issues such as Power Integrations' inequitable conduct, whether an injunction is appropriate, whether any damages should be increased, and whether this case is exceptional. Fairchild will revise identification once the Court schedules such a hearing and identifies the issues to be considered.